REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-8 remain in the application. Claims 1, 3, 6 and 7 have been amended.

In "Claim Objections", item 1 on page 2 of the above-identified Office Action, the Examiner objected to claims 3, 6 and 7 because of informalities.

More specifically, with regard to claim 3, the Examiner objected to the fact that both the first and second signals were stated as having a frequency. The Examiner expressed her opinion that the frequencies should be differentiated. It is believed that the claim was perfectly clear in its original form. There is nothing unclear about stating that the first and second signals have frequencies and then mentioning the frequencies of the first and second signals. There is no need for differentiation.

For example, if it is stated that first and second rooms have a green color, it is completely clear to later mention the green color of the rooms, without calling for first and second green colors.

Nevertheless, in order to facilitate prosecution of the instant application, claim 3 has been amended to call for the first signal having a first frequency and the second signal having a second frequency, and to later mention the first frequency of the first signal and the second frequency of the second signal.

With regard to claim 6, similarly the Examiner believes it is unclear to mention that both the first and second signals are differential signals. Once again, it is believed that the claim was perfectly clear in its original form, but to facilitate prosecution, claim 6 has been amended to call for the first signal being a first differential signal and the second signal being a second differential signal, and to later mention the first differential signal and the second differential signal.

Finally, the Examiner has objected to the wording of claims 6 and 7 and believes that the first and second signals should be renamed to differentiate the switch input signal form the switch output signal. This objection is not understood since it is not understood how an input signal referred to as input signal in the claims can be confused with an output signal referred to as an output signal in the claims. It is noted that claims 6 and 7 do not even mention the word "output."

Nevertheless, in an attempt to satisfy the Examiner's request, claim 6 has been amended to call for the first signal input including two terminals each receiving the first differential signal and the second signal input including two terminals each receiving the second differential signal. Claim 7 has been amended to call for the first switching device including a device for polarity reversal for reversing a polarity of the first input signal received by each of the two terminals of the first signal input and the second switching device including a device for polarity reversal for reversing a polarity of the second input signal received by each of the two terminals of the second signal input.

If the Examiner still has any objections to the claims, she is requested to make specific proposals to Counsel for claim amendments.

In "Claim Rejections - 35 USC § 103", item 3 on pages 3-5 of the Office Action, claims 1-8 have been rejected as being obvious over U.S. Patent No. 4,755,761 to Ray, Jr. (hereinafter Ray), under 35 U.S.C. § 103(a).

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and, therefore, the claims have not been amended to overcome the

references. However, a typographical error in claim 1 has been corrected.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, a multiplier circuit with offset compensation, comprising:

> an analog multiplier including a first signal input for receiving a first signal, a second signal input for receiving a second signal, and an output for providing a multiplied signal;
>
> **a first switching device for polarity reversal, said first switching device connected to said first signal input; and**
>
> **a second switching device for polarity reversal, said second switching device connected to said second signal input.**

Independent claim 8 contains similar language.

Accordingly, the invention of the instant application relates to a multiplier circuit with offset compensation and to a quadricorrellator having such a multiplier circuit with offset compensation.

More specifically, claim 1 of the instant application calls for a multiplier circuit with offset compensation, comprising an analog multiplier, a first switching device for polarity reversal and a second switching device for polarity reversal.

The analog multiplier has a first signal input and a second signal input, for receiving respective first and second signals. The analog multiplier further has an output for providing a multiplied signal derived from the first signal and the second signal.

It is an important aspect of the present invention that **both the first switching device for polarity reversal and the second switching device for polarity reversal are connected to signal inputs** of the multiplier circuit. According to claim 1, no switching device for polarity reversal is necessary to be provided at the output of the multiplier circuit.

One of the advantages of the configuration recited in claim 1 is that signals which are fed in at the inputs of the multiplier do not effect cross talk to the output of the analog multiplier. If a DC voltage offset remains at the output of the analog multiplier, then it will be suppressed in a simple manner by the switching devices connected to the inputs of the multiplier.

It is important to understand that no changeover switch is necessary at the output of the analog multiplier, due to the claimed structure of the multiplier circuit of the present invention. This is a result of the elimination of the

negative sign through product formation, as described in the last paragraph on page 4 of the specification of the instant application. Furthermore, between page 10, line 1 and page 11, line 2 of the specification of the instant application, it is described in detail why, according to the structure recited in claim 1, no periodic polarity reversal is necessary at the output of the multiplier.

Therefore, according to the present invention, a multiplier circuit is provided in which cross talk of input signals to the output is suppressed, with a low outlay for circuitry. The multiplier circuit can be integrated in a simple manner requiring little chip area, for example in mobile radio applications.

The Ray reference discloses a zero intermediate-frequency demodulator. More specifically, Fig. 1 of Ray shows an IF modulator 10 having an input 10a receiving a modulated signal A(t). The input is fed to first and second mixer amplifier means 11-1 and 11-2. Oscillator means 10x have a demodulator terminal 10b feeding a signal with a frequency fo to a phase-shift network 12. The network 12 feeds signals 12b, 12c to the mixer amplifier means. The mixer amplifier means feed respective in-phase and quadrature-phase signals I' and Q' to series networks 14-1, 14-2. Outputs 10c, 10d of the series

networks are fed to switch means 16 and through transfer function means 18-1, 18-2 to operation means 20-1, 20-2 for addition or multiplication. The operation means are also connected to the switch means 16. Finally, summation means 22 are connected to the operation means for supplying a demodulated output signal B(t) at an output 10e.

Ray therefore provides a zero intermediate-frequency (IF) demodulator which includes a pair of mixers receiving a quadrature local oscillator signal. The in-phase and quadrature phased signals I, Q are derived at the outputs of the two mixers in Fig. 1 of Ray. A switch 16 provides cross switching within the demodulator and is connected downstream to the mixers in the Ray circuit. The switch 16 acts as if it were a double-pole, double-throw switch having a first pole with selectable contacts S, C and having a second pole with selectable contacts S', C', which is described in detail in column 3, lines 26 to 31 of Ray.

Fig. 4 of Ray discloses two mixers 26-1 and 26-2 which are connected downstream of input mixers 11-1 and 11-2. One input of each mixer 26-1, 26-2 is directly connected to respective in-phase and quadrature phased signal nodes I, Q, while the other input is connected through delay means to the respective in-phase and quadrature phased signal nodes I, Q. The circuit

of Fig. 4 provides a cosine detector, as discussed in column 8, lines 19 to 21 of Ray.

The Examiner has admitted in the paragraph bridging pages 3 and 4 of the Office action that Ray does not teach "a first switching device for polarity reversal, said first switching device connected to said first signal input; and a second switching device for polarity reversal, said second switching device connected to said second signal input", as recited in claim 1 of the instant application.

Nevertheless, the Examiner believes that page 2, lines 23-26 of the specification of the instant application states that it is known that in order to suppress DC voltage offsets in amplifiers, the polarity of both the input signal and the output signal of the amplifier are to be periodically changed over.

However, it must be pointed out that page 2, lines 23 to 26 of the specification of the instant application refer to an amplifier, and not to a multiplier circuit. An amplifier normally has a signal input to feed in a signal to be amplified, as well as a signal output. According to what is taught on page 2 of the instant application, a person skilled in the art knows that to provide offset correction, a

switching device for polarity reversal has to be connected to the input and to the output of the amplifier.

For this reason, a person skilled in the art knowing how to provide DC correction of an amplifier and trying to provide DC offset correction in a multiplier circuit, would try to make use of his or her knowledge. What he or she knows according to page 2, lines 23 to 26 is, that at an input and at an output of the device, a periodic polarity reversal has to be implemented. When looking at Fig. 4 of Ray, the person skilled in the art recognizes that the principle taught on page 2 of the instant application can only be applied to the whole structure as presented in Fig. 4, namely to the input 10a and to the output 22c, where one input terminal and one output terminal are provided. Therefore, in order to provide an offset cancellation in the circuit of Fig. 4 of Ray, the person skilled in the art would connect a first switching device for polarity reversal to the input 10a and he or she would connect another switching device for polarity reversal to the output 22c in Fig. 4.

Both page 2 of the specification of the instant application and Ray are completely silent as to providing respective polarity reversal switching devices at two inputs of a multiplier, instead of providing one device for polarity

reversal at an input and another device for polarity reversal at an output.

Therefore, one of ordinary skill in this art, starting from Ray and trying to provide an offset cancellation device using his or her knowledge of DC cancellation in amplifiers, could not achieve a circuit having all of the features of the circuit recited in claim 1 and claim 8 of the instant application.

For this reason, it is believed that the circuits recited in claim 1 and claim 8 of the instant application are novel and non-obvious over the prior art.

Clearly, Ray does not show a first switching device for polarity reversal being connected to a first signal input and a second switching device for polarity reversal being connected to a second signal input, as recited in claims 1 and 8 of the instant application.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1 and 8. Claims 1 and 8 are, therefore, believed to be patentable over the art. The

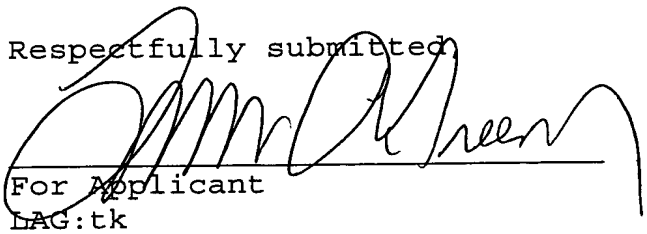
dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1.

In view of the foregoing, reconsideration and allowance of claims 1-8 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time is required, petition for extension is herewith made. Any extension fee associated therewith should be charged to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099. Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,



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